Docket No.: SON-2313
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Satoshi Ikeda

Confirmation No.: 3283

Application No.: 10/052,736

Art Unit: 2133

Filed: January 23, 2002

Examiner: J. C. Kerveros

For: SEMICONDUCTOR TESTING APPARATUS AND METHOD

REPLY BRIEF

MS Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

INTRODUCTORY COMMENTS

This is in response to the Office Action of June 17, 2005. The Office Action has made reference to rules and procedures that have been superseded and are no longer in effect. As a result, a procedural error exists within that Office Action. Specifically, page 2 of the Office Action lists a procedure for reinstatement of the appeal, citing old rule 37 C.F.R. §1.193(b)(2). However, that rule has been replaced by new rule 37 C.F.R. §41.39.

An Examiner's Answer may include a new ground of rejection. 37 C.F.R. §41.39(a)(2). Accordingly, the Office Action of June 17, 2005 is deemed to be an Examiner's Answer. Pursuant to 37 C.F.R. §41.39. This is a Reply Brief under 37 C.F.R. §41.41 in response to the Examiner's Answer mailed on June 17, 2005.

Accordingly, Appellant hereby request that the appeal be MAINTAINED by the filing this Reply Brief. See 37 C.F.R. §41.39(b)(2).

U.S. Patent and Trademark Office (USPTO) practice and procedures dictate that an appeal conference is ***mandatory*** in all cases in which an acceptable Appeal Brief has been filed. M.P.E.P. §1208. In this regard, an Appeal Brief has been filed on March 30, 2005.

The participants of the appeal conference should include (1) the examiner charged with preparation of the examiner's answer, (2) a supervisory patent examiner (SPE), and (3) another examiner, known as a conferee, having sufficient experience to be of assistance in the consideration of the merits of the issues on appeal. M.P.E.P. §1208. But while page 15 of the Examiner's Answer shows the signature of the Examiner, the Examiner's Answer fails to include the signature of the supervisory patent examiner (SPE), and the signature of another examiner as required by M.P.E.P. §1208.

As a result, clarification as to the occurrence of the mandatory appeal conference prior to the mailing of the Examiner's Answer of June 17, 2005 is respectfully requested.

All arguments presented within the Appeal Brief of March 30, 2005 are incorporated herein by reference. Additional arguments are provided hereinbelow.

Grouping of claims

Claims 3 and 6-32 are currently pending and finally rejected in this application, with claims 3, 6 and 22 being independent. For purposes of the issues presented by this appeal:

Claim 3 stands or falls alone.

Claims 6-7 and 9-10 stand or fall together.

Claim 8 stands or falls alone.

Claim 11 stands or falls alone.

Claim 12 stands or falls alone.

Claim 13 stands or falls alone.

Claim 14 stands or falls alone.

Claim 15 stands or falls alone.

Claim 16 stands or falls alone.

Claim 17 stands or falls alone.

Claim 18 stands or falls alone.

Claim 19 stands or falls alone.

Claim 20 stands or falls alone.

Claim 21 stands or falls alone.

Claim 22 stands or falls alone.

Claim 23 stands or falls alone.

Claim 24 stands or falls alone.

Claim 25 stands or falls alone.

Claim 26 stands or falls alone.

Claim 27 stands or falls alone.

Claim 28 stands or falls alone.

Claim 29 stands or falls alone.

Claim 30 stands or falls alone.

Claim 31 stands or falls alone.

Claim 32 stands or falls alone.

The arguments set forth in the following section provide reasons why these claims are considered patentable, 37 C.F.R. §41.37(c)(1)(vii).

Claim objections

The Examiner's Answer includes an objection to the claims. For the purpose of completeness, a Petition Under 37 C.F.R. § 1.181 To Request Withdrawal Of The Claim Objections is filed along with Reply Brief. Timely consideration of the Petition is respectfully requested.

Claim rejections

The Examiner erred in rejecting claim 3 under 35 U.S.C. §112, second paragraph, as allegedly being indefinite.

This rejection is traversed at least for the following reasons.

The Examiner's Answer contends that the phrase "such a manner" found within claim 3 is indefinite (Examiner's Answer at page 3).

The Examiner's Answer refers to M.P.E.P. §2173.05(d). In response, the examples found within M.P.E.P. §2173.05(d) of claim language which have been held to be indefinite are fact specific and should not be applied as *per se* rules. In this regard, the language found within filed claim 3 of "in such a manner" has not been shown within M.P.E.P. §2173.05(d) to reach the definition of indefiniteness within the meaning of 35 U.S.C. §112, second paragraph.

The Examiner's Answer contends that the phrase "such a manner" is equivalent to the phrase "such as" (Examiner's Answer at page 14).

In response to this contention, the Examiner's Answer attempts to recast the express language found within the claims. Such a reconstruction is merely an attempt to redefine the invention in a manner different than from what is set forth within the claims. Such reconstruction is without authority under Title 35 U.S.C., Title 37 C.F.R., the M.P.E.P. and relevant case law; such reconstruction is therefore deemed unusual and improper.

Page 11 of the Appeal Brief has highlighted that ***the phrase "such a manner" has been previously found by the Examiner to be acceptable claim language***. For example, the Examiner has found such claim language acceptable within claim 4 of U.S. Patent No. *6,807,644*. The Examiner has found such claim language acceptable within claim 1 of U.S. Patent No. *6,727,723*. The Examiner also has found such claim language acceptable within claims 6 and 7 of U.S. Patent No. *6,522,153*. ***Many other examples*** of the Examiner finding the term "such a manner" as acceptable claim language are within the U.S. Patent collection. Respectfully, this rejection is inconsistent with other actions taken by the Examiner.

Clarification as to why the term "such a manner" is now deemed unacceptable has been requested in the Appeal Brief (Appeal Brief at page 11). However, no clarification is found within the Examiner's Answer.

The Examiner erred in rejecting claims 3 and 6-32 under 35 U.S.C. §102 as allegedly being obvious over U.S. Patent No. 6,477,672 to Satoh in view of U.S. Patent No. 6,314,536 to Kurosaki.

This rejection is traversed at least for the following reasons.

Claim 3 - Claim 3 is drawn to a semiconductor testing apparatus wherein an input signal of a test pattern is supplied to a semiconductor device, and an output signal obtained from said semiconductor device is compared with a prescribed expected value to conduct a test, said apparatus comprising:

test pattern memory means adapted for storing test pattern data of the test pattern, managing the test pattern data in accordance with addresses, and outputting the test pattern specified by any address;

test pattern generation means for generating a test pattern signal on the basis of the test pattern outputted from said test pattern memory means; and

control means for controlling said test pattern memory means and said test pattern generation means in such a manner that the test pattern signal based on the test pattern data of a desired address can be generated at a predetermined timing conforming to the set information,

wherein said control means controls the timing of generation of the test pattern in such a manner that the cycle period rate to execute the test pattern of the desired address becomes a cycle period narrower than a predetermined rate.

Satoh arguably teaches a memory test apparatus. However, no timing diagram is found within Satoh. The Examiner's Answer ***admits*** that Satoh ***does not*** explicitly disclose *a cycle period rate to execute the test pattern of the desired address becomes a cycle period narrower than a predetermined rate* (Examiner's Answer at page 5).

The Examiner's Answer cites Kurosaki for the feature that is admittedly deficient from within Satoh. Kurosaki arguably teaches a memory testing apparatus having pattern generator 2 that generates a test pattern signal S1 applied to a device to be tested MUT 3 (column 6, lines 14-18), and a system controller 6.

The Examiner's Answer contends that Figure 5A of Kurosaki shows a test period signal Tt and Figure 5D of Kurosaki shows the burst address signals, having two burst address signals with respect to the test period signal Tt, and that the cycle period rate of Figure 5D is narrower than the test period signal Tt, by a factor of two (Examiner's Answer at page 6).

In response to this contention, Figure 5D of Kurosaki arguably teaches that the memory under test 3 produces two burst address signals in one internal clock period Tt such as ADR0 and ADR1 in the first internal clock period, and ADR2 and ADR3 in the second internal clock period (Kurosaki at column 3, 44-48).

However, *Kurosaki fails to disclose, teach, or suggest the pattern generator 2 producing the two burst address signals*. For example, in the case that the memory under test 3 operates in burst mode, an address signal which is added to the test pattern signal S1 and is applied to the memory under test 3 from the pattern generator 2 *is only one burst leading address signal* (also called the first address signal) which indicates an address of the leading or head data (the first data) in the burst, and burst address signals indicating addresses of *the second and subsequent data in the burst are automatically produced internally of the memory under test 3* in synchronism with the rising edge and the falling edge of an internal clock in the memory under test 3 (Kurosaki at column 2, lines 49-59).

As a result, Satoh and Kurosaki, either individually or as a whole, fail to disclose, teach, or suggest *a control means that controls the timing of generation of the test pattern in such a manner that the cycle period rate to execute the test pattern of the desired address becomes a cycle period narrower than a predetermined rate*.

Further note that the Examiner's Answer has identified element 100 of Satoh as the control means 100 (Examiner's Answer at page 5). When a test start instruction is given thereto from the main controller 100, the pattern generator PG outputs test pattern data to be applied to the memory under test MUT in accordance with the stored pattern generating sequence (Satoh at Figure 9, column 2, lines 28-34).

Also note that the Examiner's Answer has identified within Kurosaki a burst address producing circuit 8 (Examiner's Answer at page 5). Yet, Kurosaki fails to disclose, teach, or suggest the pattern generator 2 being controllable by the burst address producing circuit 8.

As a result, the Examiner's Answer fails to show why the skilled artisan would have been motivated to modify Satoh by replacing the main controller 100 of Satoh with the burst address producing circuit 8 of Kurosaki.

Claims 6, 7, 9, 10 - Claim 6 and the claims dependent thereon include the features of:

control means adapted to generate a timing signal and an address specifying signal, said timing signal having a test pattern cycle period, the duration of said test pattern cycle period

being variable, the rate of modification for said address specifying signal being said test pattern cycle period;

test pattern memory means adapted to store a first test pattern, said first test pattern being outputted from said test pattern memory means in response to said address specifying signal, the rate of output for said first test pattern being said test pattern cycle period; and

test pattern generation means adapted to generate an input test pattern signal by combining said first test pattern with said timing signal, a semiconductor device under test receiving said input test pattern signal.

The Examiner's Answer cites element 100 of Satoh as the control means, element 101 of Satoh as the test pattern memory means, and element PG as the test pattern generation means (Examiner's Answer at pages 6-7).

The Examiner's Answer ***admits*** that Satoh ***does not*** explicitly disclose *a variable test pattern cycle period* (Examiner's Answer at page 7).

The Examiner's Answer cites Kurosaki for the feature that is admittedly deficient from within Satoh. Kurosaki arguably teaches a memory testing apparatus having pattern generator 2 that generates a test pattern signal S1 applied to a device to be tested MUT 3 (column 6, lines 14-18), and a system controller 6.

The Examiner's Answer cites program 101 within Satoh as the test pattern (Examiner's Answer at page 7), and cites the pattern generator PG within Satoh as the test pattern generation means (Examiner's Answer at page 7). The clock-repetition-rate doubling circuit 15 of Kurosaki is additionally cited within the Examiner's Answer (Examiner's Answer at page 7).

Nevertheless, the Examiner's Answer fails to show where and how the alleged pattern generator PG of Satoh would generate an input test pattern signal by combining the program 101 of Satoh with an output from the clock-repetition-rate doubling circuit 15 of Kurosaki. In this regard, the Examiner's Answer fails to show that the skilled artisan would have been motivated to replace the pattern generator PG of Satoh with the clock-repetition-rate

doubling circuit 15 of Kurosaki when Kurosaki also teaches the presence of *its own pattern generator 2* (Kurosaki at Figure 1). Moreover, the Examiner's Answer fails to show that an output from the clock-repetition-rate doubling circuit 15 of Kurosaki would be provided as an input to the pattern generator PG of Satoh.

Thus, Satoh and Kurosaki, either individually or as a whole, fail to disclose, teach, or suggest *test pattern generation means for generating an input test pattern signal by combining the first test pattern with the timing signal, a semiconductor device under test receiving the input test pattern signal.*

Claim 8 - The rejection of claim 8 is traversed for the reasons provided hereinabove with respect to claim 6, and for the following reasons.

Within claim 8, said control means is adapted to vary said duration of said test pattern cycle period.

The Examiner's Amendment cites controller 100 of Satoh as the control means. However, the Examiner's Amendment admits that Satoh fails to disclose, teach, or suggest control means is adapted to vary said duration of said test pattern cycle period.

Moreover, Kurosaki fails to show that the system controller 6 is adapted to vary the duration of the test pattern cycle period. Specifically, Kurosaki arguably teaches that the reference clock is given to the burst address producing circuit 8 as *a test period signal TI* for defining one test period or cycle in the memory testing apparatus 1 (Kurosaki at column 6, lines 48-51). In addition, Figures 2E, 3D, and 5A of Kurosaki fail to show a variance in the test period signal TI.

Claim 11 - The rejection of claim 11 is traversed for the reasons provided hereinabove with respect to claim 6, and for the following reasons.

Claim 11 includes said control means receiving set information to generate said timing signal and said address specifying signal, said set information establishing said duration of said test pattern cycle period.

The Examiner's Answer ***admits*** that Satoh ***does not*** explicitly disclose *a variable test pattern cycle period* (Examiner's Answer at page 7).

Kurosaki arguably teaches that the reference clock is given to the burst address producing circuit 8 as *a test period signal TI* for defining one test period or cycle in the memory testing apparatus 1 (Kurosaki at column 6, lines 48-51).

However, the Kurosaki fails to show that the system controller 6 receives set information to generate the timing signal TI. Instead, a timing generator 7 supplies a reference clock to the pattern generator 2 and the system controller 6 respectively (Kurosaki at column 6, lines 11-13).

In addition, Kurosaki fails to disclose, teach, or suggest the use of set information to generate the address specifying signal. Moreover, Kurosaki fails to disclose, teach, or suggest set information that establishes the duration of the test pattern cycle period.

Claim 12 - The rejection of claim 12 is traversed for the reasons provided hereinabove with respect to claim 11, and for the following reasons.

Within claim 12 said control means controls the timing of generation of said first test pattern on the basis of said set information.

The Examiner's Answer ***admits*** that Satoh ***does not*** explicitly disclose *a variable test pattern cycle period* (Examiner's Answer at page 7).

Kurosaki fails to disclose, teach, or suggest the system controller 6 as controlling the timing of generation of a test pattern. Instead, the pattern generator 2 of Kurosaki arguably generates, in response to the reference clock supplied thereto from the timing generator 7, an address signal, a test signal of a predetermined pattern (a test pattern signal) S1 and a control signal which are to be supplied to an IC memory to be tested or under test 3 (commonly called MUT) (Kurosaki at column 6, lines 19-25).

In addition, Kurosaki fails to disclose, teach, or suggest the system controller 6 as controlling the timing of generation of a test pattern on the basis of set information.

Claim 13 - The rejection of claim 13 is traversed for the reasons provided hereinabove with respect to claim 11, and for the following reasons.

Within claim 13, said test pattern cycle period is narrowed by varying said set information.

The Examiner's Answer ***admits*** that Satoh ***does not*** explicitly disclose that the test pattern cycle period is narrowed by varying said set information (Examiner's Answer at page 11).

In addition, Figures 2E, 3D, and 5A of Kurosaki fail to show a variance in the test period signal TI.

Claim 14 - The rejection of claim 14 is traversed for the reasons provided hereinabove with respect to claim 11, and for the following reasons.

Within claim 14, said test pattern cycle period is widened by varying said set information.

The Examiner's Answer ***admits*** that Satoh ***does not*** explicitly disclose that the test pattern cycle period is widened by varying said set information.

In addition, Figures 2E, 3D, and 5A of Kurosaki fail to show a variance in the test period signal TI.

Claim 15 - The rejection of claim 15 is traversed for the reasons provided hereinabove with respect to claim 6, and for the following reasons.

Within claim 15, said test pattern memory means stores a plurality of test patterns, said plurality of test patterns being outputted from said test pattern memory means in response to said address specifying signal, the rate of output for said plurality of test patterns being said test pattern cycle period.

The Examiner's Answer ***admits*** that Satoh ***does not*** explicitly disclose *a variable test pattern cycle period* (Examiner's Answer at page 7).

While Kurosaki arguably teaches that the pattern generator 2 generates a test signal of *a predetermined pattern* (a test pattern signal) S1 (Kurosaki at column 6, lines 14-18), Kurosaki fails to disclose, teach, or suggest test pattern memory means that stores a plurality of test patterns.

Claim 16 - The rejection of claim 16 is traversed for the reasons provided hereinabove with respect to claim 15, and for the following reasons.

Within claim 16, said duration of said test pattern cycle period only for said first test pattern is narrowed.

The Examiner's Answer ***admits*** that Satoh ***does not*** explicitly disclose that the duration of said test pattern cycle period only for the first test pattern is narrowed (Examiner's Answer at page 12).

Figures 2E, 3D, and 5A of Kurosaki fail to show a variance in the test period signal TI. Thus, Kurosaki fails to disclose, teach, or suggest that the duration of said test pattern cycle period only for the first test pattern is narrowed. Moreover, Kurosaki fails to teach a treatment only for the first test pattern.

Claim 17 - The rejection of claim 17 is traversed for the reasons provided hereinabove with respect to claim 15, and for the following reasons.

Within claim 17, said duration of said test pattern cycle period for said first test pattern and for said plurality of test patterns is narrowed.

The Examiner's Answer ***admits*** that Satoh ***does not*** explicitly disclose that the duration of said test pattern cycle period only for the first test pattern is narrowed (Examiner's Answer at page 12).

Figures 2E, 3D, and 5A of Kurosaki fail to show a variance in the test period signal TI. Thus, Kurosaki fails to disclose, teach, or suggest that the duration of said test pattern cycle period for the first test pattern and for the plurality of test patterns is narrowed. Moreover, Kurosaki fails to teach a treatment only for the first test pattern.

While Kurosaki arguably teaches that the pattern generator 2 generates a test signal of *a predetermined pattern* (a test pattern signal) S1 (Kurosaki at column 6, lines 14-18), Kurosaki fails to disclose, teach, or suggest test pattern memory means that stores a plurality of test patterns.

Claim 18 - The rejection of claim 18 is traversed for the reasons provided hereinabove with respect to claim 15, and for the following reasons.

Within claim 18, said duration of said test pattern cycle period for said plurality of test patterns is narrowed successively from the top pattern address throughout the entire test pattern in order.

The Examiner's Answer ***admits*** that Satoh ***does not*** explicitly disclose that the duration of said test pattern cycle period only for the first test pattern is narrowed (Examiner's Answer at page 12).

Figures 2E, 3D, and 5A of Kurosaki fail to show a variance in the test period signal TI. Thus, Kurosaki fails to disclose, teach, or suggest that the duration of the test pattern cycle period for the plurality of test patterns is narrowed successively from the top pattern address throughout the entire test pattern in order.

Moreover, while Kurosaki arguably teaches that the pattern generator 2 generates a test signal of *a predetermined pattern* (a test pattern signal) S1 (Kurosaki at column 6, lines 14-18), Kurosaki fails to disclose, teach, or suggest test pattern memory means that stores a plurality of test patterns.

Claim 19 - The rejection of claim 19 is traversed for the reasons provided hereinabove with respect to claim 15, and for the following reasons.

Within claim 19, said duration of said test pattern cycle period only for said first test pattern is widened.

The Examiner's Answer ***admits*** that Satoh ***does not*** explicitly disclose that the duration of the test pattern cycle period only for the first test pattern is widened (Examiner's Answer at page 13).

Figures 2E, 3D, and 5A of Kurosaki fail to show a variance in the test period signal TI. Thus, Kurosaki fails to disclose, teach, or suggest that the duration of the test pattern cycle period only for the first test pattern is widened. Moreover, Kurosaki fails to teach a treatment only for the first test pattern.

Claim 20 - The rejection of claim 20 is traversed for the reasons provided hereinabove with respect to claim 15, and for the following reasons.

Within claim 20, said duration of said test pattern cycle period for said first test pattern and for said plurality of test patterns is widened.

The Examiner's Answer ***admits*** that Satoh ***does not*** explicitly disclose that the duration of the test pattern cycle period only for the first test pattern is widened (Examiner's Answer at page 13).

Figures 2E, 3D, and 5A of Kurosaki fail to show a variance in the test period signal TI. Thus, Kurosaki fails to disclose, teach, or suggest that the duration of the test pattern cycle period for the first test pattern and for the plurality of test patterns is widened.

Moreover, while Kurosaki arguably teaches that the pattern generator 2 generates a test signal of *a predetermined pattern* (a test pattern signal) S1 (Kurosaki at column 6, lines 14-18), Kurosaki fails to disclose, teach, or suggest test pattern memory means that stores a plurality of test patterns.

Claim 21 - The rejection of claim 21 is traversed for the reasons provided hereinabove with respect to claim 15, and for the following reasons.

Within claim 21, said duration of said test pattern cycle period for said plurality of test patterns is widened successively from the top pattern address throughout the entire test pattern in order.

The Examiner's Answer ***admits*** that Satoh ***does not*** explicitly disclose that the duration of the test pattern cycle period only for the first test pattern is widened (Examiner's Answer at page 13).

Figures 2E, 3D, and 5A of Kurosaki fail to show a variance in the test period signal TI. Thus, Kurosaki fails to disclose, teach, or suggest that the duration of the test pattern cycle period for the plurality of test patterns is widened successively from the top pattern address throughout the entire test pattern in order.

Claim 22 - Claim 22 and the claims dependent thereon include the steps of:

generating a timing signal having a test pattern cycle period;

varying the duration of said test pattern cycle period;

generating an address specifying signal, the rate of modification for said address specifying signal being said test pattern cycle period;

storing a first test pattern within test pattern memory means;

outputting said first test pattern from within test pattern memory means in response to said address specifying signal, the rate of output for said first test pattern being said test pattern cycle period;

combining said first test pattern with said timing signal to generate an input test pattern signal, a semiconductor device under test receiving said input test pattern signal; and

comparing an output test pattern signal from said semiconductor device under test with said first test pattern.

The Examiner's Answer cites element 100 of Satoh as the control means, element 101 of Satoh as the test pattern memory means, and element PG as the test pattern generation means (Examiner's Answer at pages 6-7).

The Examiner's Answer ***admits*** that Satoh ***does not*** explicitly disclose *varying the test pattern cycle period* (Examiner's Answer at page 9).

The Examiner's Answer cites Kurosaki for the feature that is admittedly deficient from within Satoh. Kurosaki arguably teaches a memory testing apparatus having pattern generator 2 that generates a test pattern signal S1 applied to a device to be tested MUT 3 (column 6, lines 14-18), and a system controller 6.

The Examiner's Answer cites program 101 within Satoh as the test pattern (Examiner's Answer at page 9), and cites the pattern generator PG within Satoh as the test pattern generation means (Examiner's Answer at page 9). The clock-repetition-rate doubling circuit 15 of Kurosaki is additionally cited within the Examiner's Answer (Examiner's Answer at page 9).

Nevertheless, the Examiner's Answer fails to show where and how the alleged pattern generator PG of Satoh would generate an input test pattern signal by combining the program 101 of Satoh with an output from the clock-repetition-rate doubling circuit 15 of Kurosaki. In this regard, the Examiner's Answer fails to show that the skilled artisan would have been motivated to replace the pattern generator PG of Satoh with the clock-repetition-rate doubling circuit 15 of Kurosaki when Kurosaki also teaches the presence of *its own pattern generator 2* (Kurosaki at Figure 1). Moreover, the Examiner's Answer fails to show that an output from the clock-repetition-rate doubling circuit 15 of Kurosaki would be provided as an input to the pattern generator PG of Satoh.

Thus, Satoh and Kurosaki, either individually or as a whole, fail to disclose, teach, or suggest *test pattern generation means for generating an input test pattern signal by combining the first test pattern with the timing signal, a semiconductor device under test receiving the input test pattern signal.*

Claim 23 - The rejection of claim 23 is traversed for the reasons provided hereinabove with respect to claim 22, and for the following reasons.

Claim 23 includes the additional steps of receiving set information to generate said timing signal and said address specifying signal; and using said set information to establish said duration of said test pattern cycle period.

The Examiner's Answer ***admits*** that Satoh ***does not*** explicitly disclose *a variable test pattern cycle period* (Examiner's Answer at page 9).

Kurosaki arguably teaches that the reference clock is given to the burst address producing circuit 8 as *a test period signal TI* for defining one test period or cycle in the memory testing apparatus 1 (Kurosaki at column 6, lines 48-51).

However, the Kurosaki fails to show that the system controller 6 receives set information to generate the timing signal TI. Instead, a timing generator 7 supplies a reference clock to the pattern generator 2 and the system controller 6 respectively (Kurosaki at column 6, lines 11-13).

In addition, Kurosaki fails to disclose, teach, or suggest the use of set information to generate the address specifying signal. Moreover, Kurosaki fails to disclose, teach, or suggest set information that establishes the duration of the test pattern cycle period.

Claim 24 - The rejection of claim 24 is traversed for the reasons provided hereinabove with respect to claim 23, and for the following reasons.

Within claim 24, said test pattern cycle period is narrowed by varying said set information.

The Examiner's Answer ***admits*** that Satoh ***does not*** explicitly disclose that the test pattern cycle period is narrowed by varying said set information (Examiner's Answer at page 11).

In addition, Figures 2E, 3D, and 5A of Kurosaki fail to show a variance in the test period signal TI.

Claim 25 - The rejection of claim 25 is traversed for the reasons provided hereinabove with respect to claim 23, and for the following reasons.

Within claim 25, said test pattern cycle period is widened by varying said set information.

The Examiner's Answer ***admits*** that Satoh ***does not*** explicitly disclose that the test pattern cycle period is widened by varying said set information.

In addition, Figures 2E, 3D, and 5A of Kurosaki fail to show a variance in the test period signal TI.

Claim 26 - The rejection of claim 26 is traversed for the reasons provided hereinabove with respect to claim 22, and for the following reasons.

Within claim 26, said test pattern memory means stores a plurality of test patterns, said plurality of test patterns being outputted from said test pattern memory means in response to said address specifying signal, the rate of output for said plurality of test patterns being said test pattern cycle period.

The Examiner's Answer ***admits*** that Satoh ***does not*** explicitly disclose *a variable test pattern cycle period* (Examiner's Answer at page 9).

While Kurosaki arguably teaches that the pattern generator 2 generates a test signal of *a predetermined pattern* (a test pattern signal) S1 (Kurosaki at column 6, lines 14-18), Kurosaki fails to disclose, teach, or suggest test pattern memory means that stores a plurality of test patterns.

Claim 27 - The rejection of claim 27 is traversed for the reasons provided hereinabove with respect to claim 22, and for the following reasons.

Within claim 27, said duration of said test pattern cycle period only for said first test pattern is narrowed.

The Examiner's Answer ***admits*** that Satoh ***does not*** explicitly disclose that the duration of said test pattern cycle period only for the first test pattern is narrowed (Examiner's Answer at page 12).

Figures 2E, 3D, and 5A of Kurosaki fail to show a variance in the test period signal TI. Thus, Kurosaki fails to disclose, teach, or suggest that the duration of said test pattern cycle period only for the first test pattern is narrowed. Moreover, Kurosaki fails to teach a treatment only for the first test pattern.

Claim 28 - The rejection of claim 28 is traversed for the reasons provided hereinabove with respect to claim 22, and for the following reasons.

Within claim 28, said duration of said test pattern cycle period for said first test pattern and for said plurality of test patterns is narrowed.

The Examiner's Answer ***admits*** that Satoh ***does not*** explicitly disclose that the duration of said test pattern cycle period only for the first test pattern is narrowed (Examiner's Answer at page 12).

Figures 2E, 3D, and 5A of Kurosaki fail to show a variance in the test period signal TI. Thus, Kurosaki fails to disclose, teach, or suggest that the duration of said test pattern cycle period for the first test pattern and for the plurality of test patterns is narrowed. Moreover, Kurosaki fails to teach a treatment only for the first test pattern.

While Kurosaki arguably teaches that the pattern generator 2 generates a test signal of *a predetermined pattern* (a test pattern signal) S1 (Kurosaki at column 6, lines 14-18), Kurosaki fails to disclose, teach, or suggest test pattern memory means that stores a plurality of test patterns.

Claim 29 - The rejection of claim 29 is traversed for the reasons provided hereinabove with respect to claim 22, and for the following reasons.

Within claim 29, said duration of said test pattern cycle period for said plurality of test patterns is narrowed successively from the top pattern address throughout the entire test pattern in order.

The Examiner's Answer ***admits*** that Satoh ***does not*** explicitly disclose that the duration of said test pattern cycle period only for the first test pattern is narrowed (Examiner's Answer at page 12).

Figures 2E, 3D, and 5A of Kurosaki fail to show a variance in the test period signal TI. Thus, Kurosaki fails to disclose, teach, or suggest that the duration of the test pattern cycle period for the plurality of test patterns is narrowed successively from the top pattern address throughout the entire test pattern in order.

Moreover, while Kurosaki arguably teaches that the pattern generator 2 generates a test signal of *a predetermined pattern* (a test pattern signal) S1 (Kurosaki at column 6, lines 14-18), Kurosaki fails to disclose, teach, or suggest test pattern memory means that stores a plurality of test patterns.

Claim 30 - The rejection of claim 30 is traversed for the reasons provided hereinabove with respect to claim 22, and for the following reasons.

Within claim 30, said duration of said test pattern cycle period only for said first test pattern is widened.

The Examiner's Answer ***admits*** that Satoh ***does not*** explicitly disclose that the duration of the test pattern cycle period only for the first test pattern is widened (Examiner's Answer at page 13).

Figures 2E, 3D, and 5A of Kurosaki fail to show a variance in the test period signal TI. Thus, Kurosaki fails to disclose, teach, or suggest that the duration of the test pattern cycle period only for the first test pattern is widened. Moreover, Kurosaki fails to teach a treatment only for the first test pattern.

Claim 31 - The rejection of claim 31 is traversed for the reasons provided hereinabove with respect to claim 22, and for the following reasons.

Within claim 31, said duration of said test pattern cycle period for said first test pattern and for said plurality of test patterns is widened.

The Examiner's Answer ***admits*** that Satoh ***does not*** explicitly disclose that the duration of the test pattern cycle period only for the first test pattern is widened (Examiner's Answer at page 13).

Figures 2E, 3D, and 5A of Kurosaki fail to show a variance in the test period signal TI. Thus, Kurosaki fails to disclose, teach, or suggest that the duration of the test pattern cycle period for the first test pattern and for the plurality of test patterns is widened.

Moreover, while Kurosaki arguably teaches that the pattern generator 2 generates a test signal of *a predetermined pattern* (a test pattern signal) S1 (Kurosaki at column 6, lines 14-18), Kurosaki fails to disclose, teach, or suggest test pattern memory means that stores a plurality of test patterns.

Claim 32 - The rejection of claim 32 is traversed for the reasons provided hereinabove with respect to claim 22, and for the following reasons.

Within claim 32, said duration of said test pattern cycle period for said plurality of test patterns is widened successively from the top pattern address throughout the entire test pattern in order.

The Examiner's Answer ***admits*** that Satoh ***does not*** explicitly disclose that the duration of the test pattern cycle period only for the first test pattern is widened (Examiner's Answer at page 13).

Figures 2E, 3D, and 5A of Kurosaki fail to show a variance in the test period signal TI. Thus, Kurosaki fails to disclose, teach, or suggest that the duration of the test pattern cycle period for the plurality of test patterns is widened successively from the top pattern address throughout the entire test pattern in order.

Moreover, while Kurosaki arguably teaches that the pattern generator 2 generates a test signal of *a predetermined pattern* (a test pattern signal) S1 (Kurosaki at column 6, lines 14-18), Kurosaki fails to disclose, teach, or suggest test pattern memory means that stores a plurality of test patterns. In addition, Kurosaki fails to disclose, teach, or suggest the widening of a test pattern.

Conclusion

Therefore, a reversal of the rejection of June 17, 2005 is respectfully requested. If any fee is required or any overpayment made, the Commissioner is hereby authorized to charge the fee or credit the overpayment to Deposit Account # 18-0013.

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Respectfully submitted,

By _____
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